Terasic Technologies

DE1-SoC Development Kit







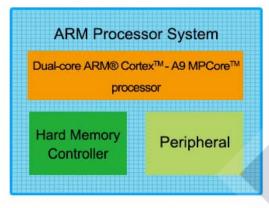
Altera DE1-SoC





SoC FPGA!









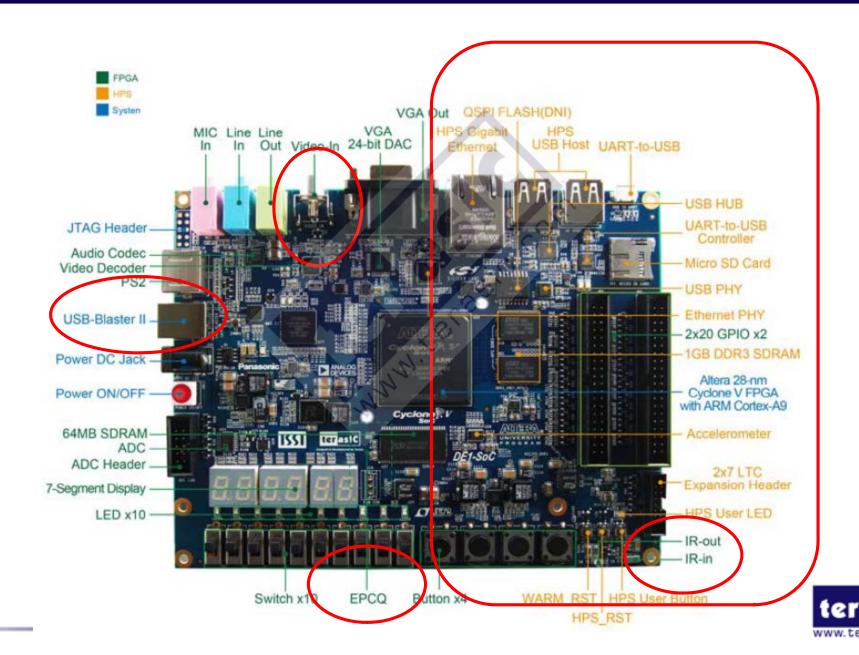


ARM + Altera = SoC FPGA



DE1-SoC Features

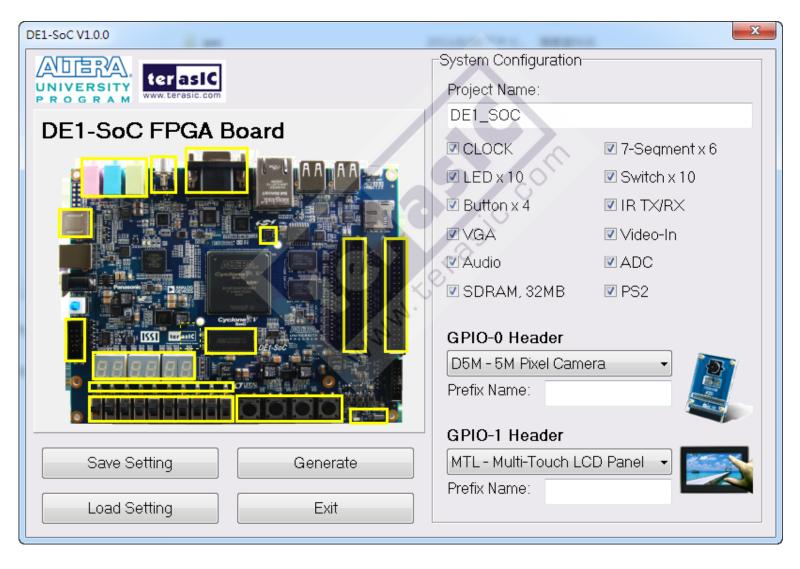
DE1-SoC Board View – Function



Utility and Resource

System Builder

• Create Quartus golden top, including various GPIO daughter boards





Linux BSP (Board Support Package)

- Linux kernel 3.12 with support of Ethernet, UART, SD/MMC, GPIO and SDRAM
- U-boot version 2013.0101 with support of Ethernet, UART, SD/MMC and SDRAM
- Yocto version 'Danny'
- Preloader
- Root file system

```
COM12 - PuTTY
                                                                      devtmpfs: mounted
Freeing init memory: 168K
INIT: version 2.88 booting
Starting Bootlog daemon: bootlogd.
Configuring network interfaces... eth0: device MAC address 6e:78:d7:d1:79:f4
udhcpc (v1.20.2) started
Sending discover...
Sending discover...
Sending discover ...
No lease, failing
Starting portmap daemon...
INIT: Entering runlevel: 5
Starting OpenBSD Secure Shell server: sshd
NET: Registered protocol family 10
IPv6: ADDRCONF(NETDEV UP): eth0: link is not ready
done.
Starting syslogd/klogd: done
Starting Lighttpd Web Server: lighttpd.
Stopping Bootlog daemon: bootlogd.
Poky 8.0 (Yocto Project 1.3 Reference Distro) 1.3 socfpga cyclone5 ttyS0
socfpga cyclone5 login: croot
root@socfpga cyclone5:~#
```

Download form Terasic Website

DE1-SoC Board

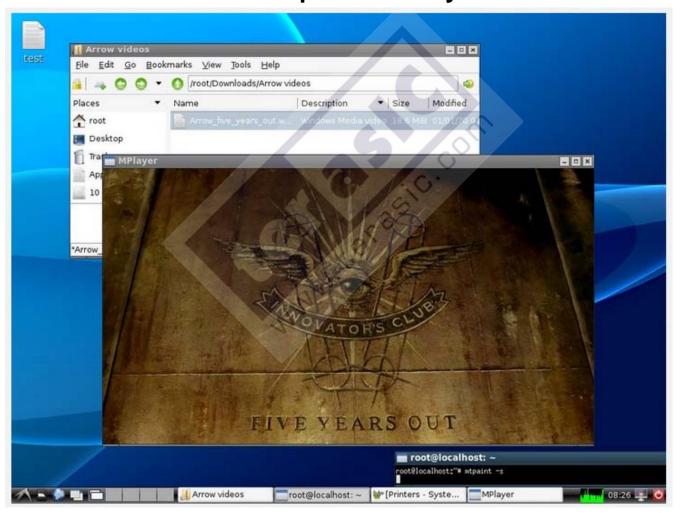
Linux BSP (Board Support Package): MicroSD Card Image

Title	Linux Kernel	Min. micro SD Capacity	Size(KB)	Date Added	Download
Linux Console	3,12	4GB	66495	2014-01-14	
Linux Console with framebuffer	3.12	AGB	328524	2014-03-24	
Linux LXDE Desktop	3.12	8GB	1369526	2014-03-21	
Linux Ubuntu Desktop	3.12	8GB	1136075	2014-02-11	



Desktop Linux Supporting

- Desktop ready for DE1-SoC: LXDE (Lightweight X11 Desktop Environment)
- Display Scheme: frame buffer is implemented by FPGA + DDR3 + Altera VIP





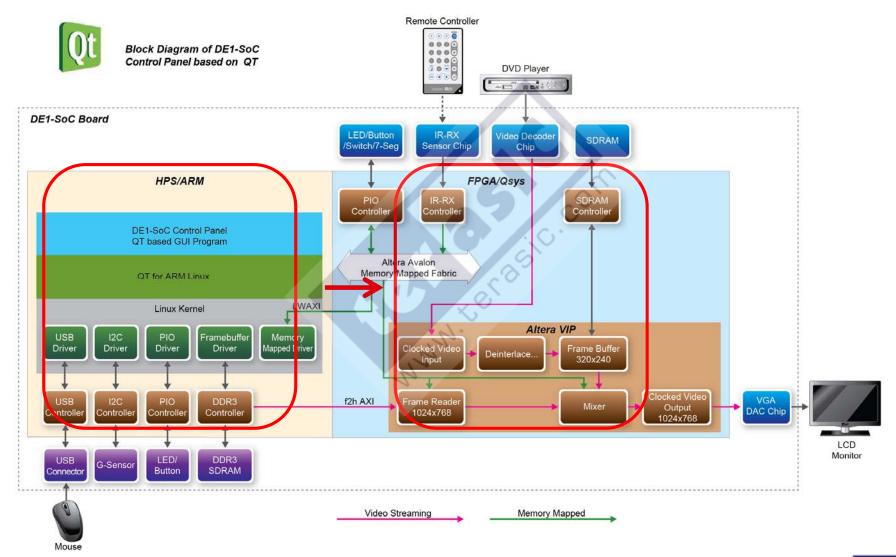
Control Panel on Linux

- HPS Control FPGA device
- Base on QT





Block Diagram of Control Panel





Daughter Card

GPIO Interface:

- MTL:
 - 7" LCD, 800x480 pixel, 24-bits color
 - Multi-touch Gesture
- D5M: 5 Mega Pixel Camera
- ADA: High speed
 - 14-bit 65 MSPS A/D
 - 14-bit 125 MSPS D/A
- LTC Interface
 - DC934A: 20-bit A/D, 16-bit D/A



Expansion



DE1-SoC + MTL

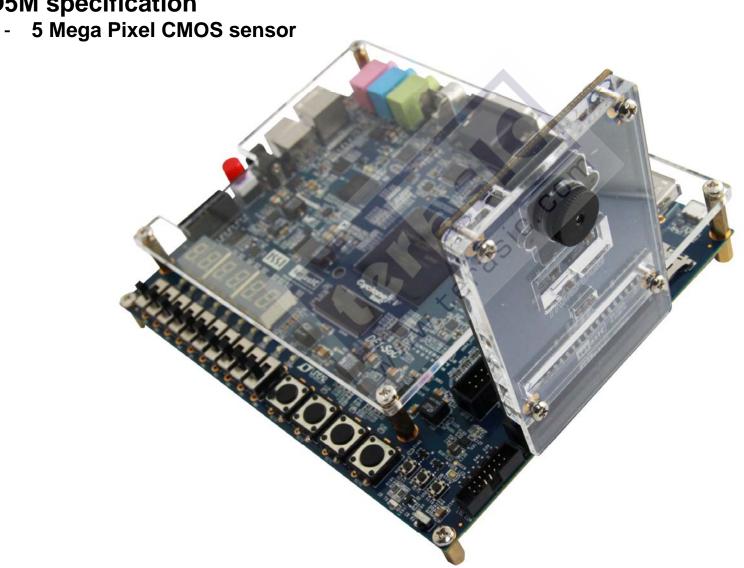
- Will support Android developed by Fujisoft
- MTL specification:
 - 7" LCD, 800x480 pixels, 24-bit color
 - Multi-touch Gesture





DE1-SoC + D5M

• D5M specification





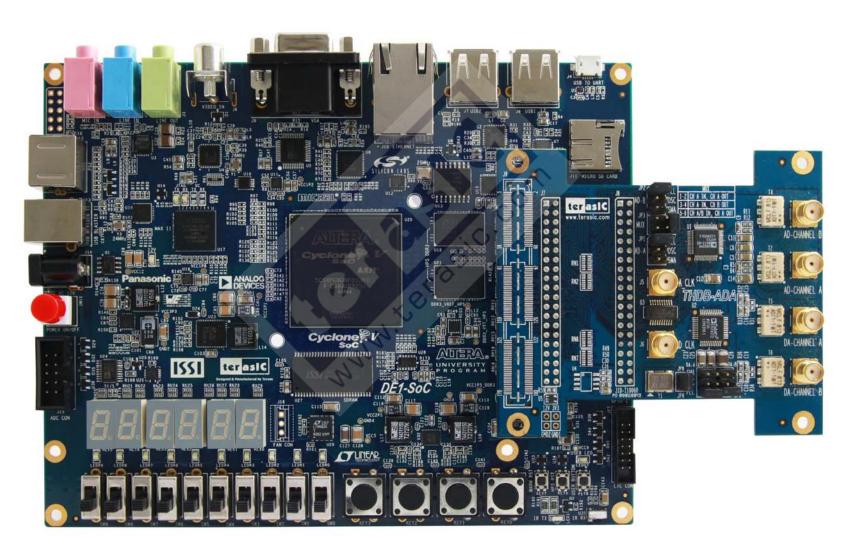
DE1-SoC + D5M + MTL





DE1-SoC + ADA

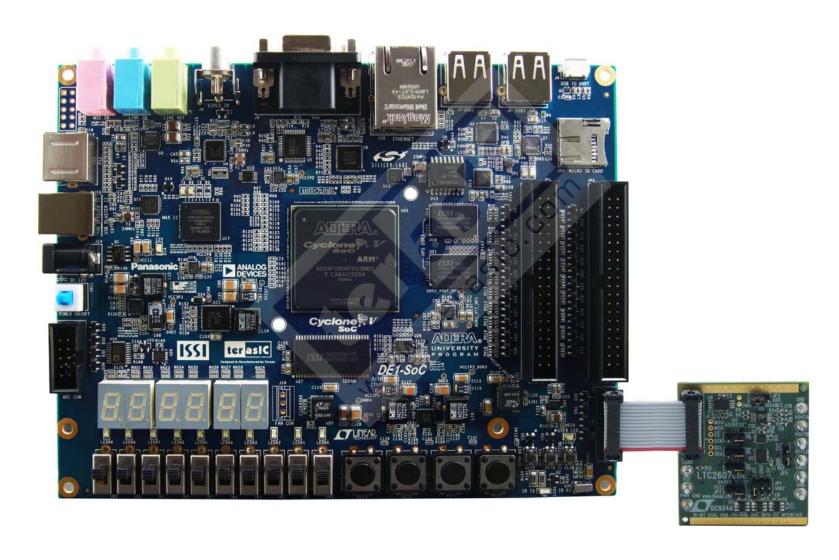
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DE1-SoC + LTC DC934A

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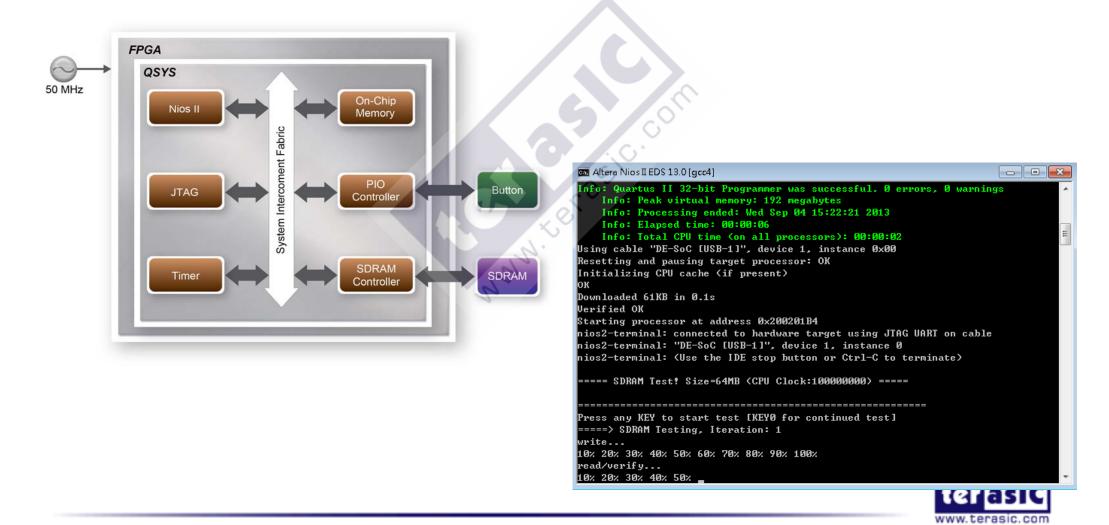


Demo



FPGA Demo

 We describe how the Altera's SDRAM Controller IP is used to access a SDRAM, and how the Nios II processor is used to read and write the SDRAM for hardware verification.



Software Development

- Development Kits
- How to control the controllers in HPS
- How to communicate with FPGA
- HPS reconfigure FPGA



Linux Demo

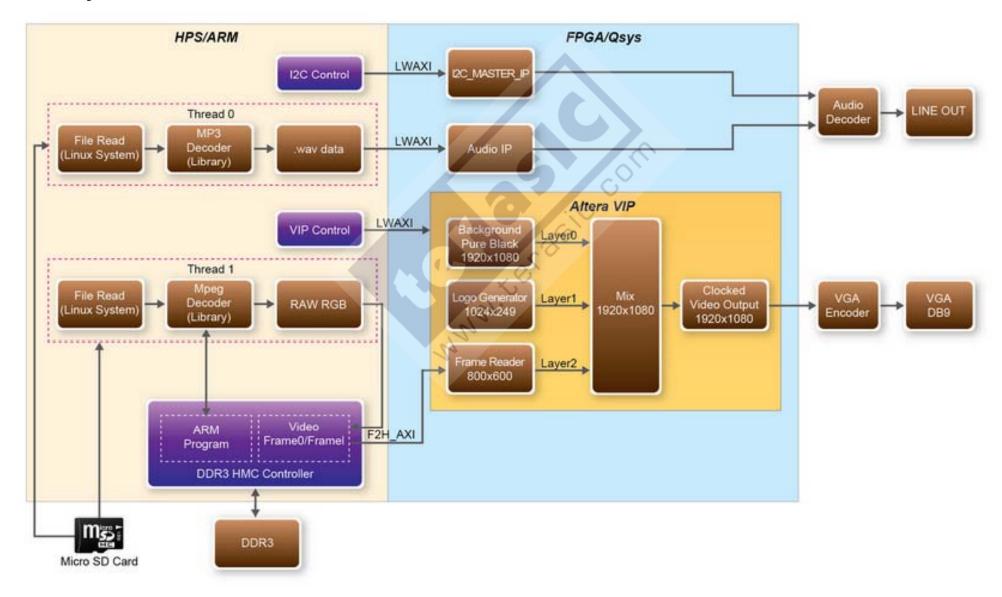
- Decode MP3/MPG and Play
- Linux with X-Windows
- Android





HPS-FPGA Demo on DE1-SoC

Play MP3 and MPEG File



Coming



Android Supporting

- Fujisoft company provides the Graphics Accelerator IP Core needed to run Android OS smoothly.
- AUP in U.T are working on porting Android too.





More Resources

More Resources on Rockbaord.org

Vist: http://www.rocketboards.org/foswiki/Main/WebHome

